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PRACTICAL CHIP DESIGN



EDN Executive Editor Ron Wilson explores how IC design teams really work: the struggle for power efficiency and performance, wrestling with semiconductor processes and design methodologies, the challenges of global design teams. How do we somehow herd architecture, IP, design and verification into a successful tape-out?

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Methodics pushes software-developers' software configuration management as cure for chip design

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The data-management problems in IC design and those in software development have superficial similarities, even though the steps in the two development processes are quite different. Both require the design management to maintain a database with multiple views of each design object, to allow authorized check-out and check-in of data, and to manage workflow across a fragmented global design team. Both have the same data-management level problems of maintaining coherency of a single approved design, allowing rapid inspection and incorporation of proposed changes, supporting design reviews, and, periodically, building a release version of the design as it then stands.

In the software development world, these management activities have for years been handled by Software Configuration Management (SCM) tools. Beginning with commercial offerings even before the early UNIX tools for comparing, merging, and versioning software, tool vendors addressed the problem explicitly. Today in the software world there are two primary environments for SCM, Subversion and Perforce, each surrounded by an extensive infrastructure of utilities.

But in the chip-design world, with a couple of exceptions such as the old Synchronicity tools, data management has been rather ad-hoc. Every management team had to do it, but each had to decide on its own approach. As chip design becomes more like software design, and in particular as SoC projects become dominated by tightly-coupled software development efforts, perhaps it makes sense to borrow some tools from the software world.

At least that's the thinking behind **MethodICs'** product VersIC. VersIC is essentially a bridge. One end of the bridge is anchored in the Cadence Virtuoso/Composer environment, while the other rests in your choice of either the Subversion or Perforce SCM database. When a user creates, opens, or modifies a design object in the Cadence custom environment, VersIC generates the correct commands to the SCM system to fulfill the data requests.

Communication to the SCM world is via either streaming or statefull TCP/IP,

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depending on your choice of database, rather than the slower and bottleneck-prone Network File System. And VersiC supports local repositories, so while a remote site is working on a piece of the design they can keep a local copy of the current data, reducing the impact of global Internet latencies on the work without sacrificing design coherency.

In addition to this bridging function, MethodICs is now adding plug-in design management tools to VersiC. The first of these, which company cofounder Simon Butler said has been in the field for some time now, is MergeIC. This plug-in has two functions. First, it shows visually in the Cadence environment the differences between two versions of a cell, at either the Verilog-A, schematic, or layout level. The tool is topology-aware, understands the Cadence design hierarchy, and allows explicit tracking of ECOs as part of the difference-viewing process. The second function, as the name suggests, is a merge capability that merges approved changes back into the SCM database.

The second tool, ReviewiC, allows managers to in effect conduct a design review across multiple remote design teams via e-mail-like threads. Based on a monitoring Web site, ReviewiC allows participants to visually browse design views, highlight and annotate objects, create and track action items associated with the design objects, and associate a proposed design change to a specific action item when the change is checked into the SCM database.

Rather than requiring live participation—meaning someone somewhere in the world has to be on-line at 0200—ReviewiC can function as a series of threads, generated in one location and then posted to the mailboxes in other locations. The tool tracks these threads, and reports when they are opened, what actions are taken, and so on. Thus the tool does the rudiments of a workflow management system in addition to providing a visual front-end for discussing design data. All of the work-flow tracking is done via a separate Light mySQL database.

Just how effective MethodICs can be in getting design teams to adopt a commercial solution to the design version-control problem remains to be seen. There are a lot of headstones sticking up in this field. But it seems very reasonable to try at least to exploit the huge base of user experience and utility infrastructure that has grown up around SCM. And it certainly seems reasonable eventually to strive for a unified chip-design/software-development version-control database, as the IC work and the software become more and more inextricably linked, both in design and in verification.

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