

PALLAB'S PLACE

EDA and Semiconductor Insights



SEARCH

CATEGORIES

- [General](#) (6)
- [Uncategorized](#) (48)

MONTHLY

- [August 2009](#) (1)
- [July 2009](#) (5)
- [June 2009](#) (3)
- [May 2009](#) (3)
- [April 2009](#) (4)
- [February 2009](#) (5)
- [January 2009](#) (2)
- [December 2008](#) (2)
- [November 2008](#) (2)
- [October 2008](#) (3)
- [September 2008](#) (3)
- [August 2008](#) (3)
- [July 2008](#) (1)
- [June 2008](#) (2)
- [May 2008](#) (4)
- [April 2008](#) (3)
- [October 2007](#) (2)
- [July 2007](#) (3)
- [June 2007](#) (1)
- [November 2006](#) (1)

PAGES

- [About](#)
- [IEEE Nanotechnology Symposium 2009, Energy and Applications](#)
- [IEEE Nanotechnology - Enabling Energy Efficiency Preview](#)
- [Samsung Secure SSD Drives - RSA 2009](#)

DAC 2009 - Methodics, Lynguent, Tela Innovation, TSMC PDKs

Published by [admin](#) at 12:31 am under [Uncategorized](#)

Aug
06
2009

Continuing the diversity of tool vendors at DAC, Methodics was showing their Data Management (DM) tools. The product is targeted at supporting a Diff/Merge function on the design data in a Cadence 5.1 and 6.1 design environment. The core of their tool is a change and revision control manager that are based in the software industry. Their current product can use either SubVersion or PerForce as revision and build engines, and they are working on a ClearCase version. These products support Revision Control (RCS) and also branch and merge on the data formats, this group of functions is called Data Management (DM) in the Methodic terminology.

The tool is targeted towards supporting remote design reviews as a collaboration tool. To support this function, the database contains only links to design objects and there is no proprietary metadata involved. With the assumption that the customer already has a core license for SubVersion/PerForce/or ClearCase, the Methodics licenses are available on a per version/per user/per year basis.

Lynguent introduced a major modeling enhancement to their environment - interface directly to the Simulink environment in addition to the existing MAST models. Their product is a modeling tool only and is simulator agnostic, so it works with most SPICE and High Capacity simulators. It also has an integration with the Cadence design environment versions 5.1 and 6.1. The resulting models behavioral models for the blocks in either Verilog A, Verilog AMS or VHDL AMS format.

The new version of the tool has a topology editor for the subsections of the circuits that identify functions such as filters, gain stages, etc. These help create the signal flow model for the blocks and describe the event dynamics in both signal slope and time domain response. When used in the mode for Rad Hard by Design, the resulting HDL model is not just post dose degradation effects of the single devices, rather it includes adjacent device ionization effects. This is a key enhancement for memory designs and bus based designs that are trying to analyze SEE effects.

The new version supports hierarchical design construction, but does not require the inside of the Verilog block to keep the hierarchical order.

Tela Innovation was showing some aspects of their relationship with TSMC on advanced libraries.

After the acquisition of Blaze DFM, Tela is expanding their IP & royalty model with TSMC. The Blaze product and service is branded as "Power Trim" and focuses on post layout power optimization.

The Tela library product and service is branded as "Area Trim". Their design architecture, when applied to standard rules on existing processes result in a smaller aggregated block size for a function cell. This reduced cell size is based on creating a "slim" library with only device level (diffusion, contact, poly, implant) changes [FEOL] and does not affect the metal pattern or pin locations for the block. This reduced cell size helps improve the yield of the design.

TSMC introduced their iPDK libraries as part of their direction for design support on 65nm and smaller processes. The iPDK libraries are core only libraries that have traditional fixed hard I/O cells which incorporate the pads and the ESD devices. These PDKs supplement the iRCx and iDRC tool independent flows that are already in place. Their iLVS kits are in progress. An iDFM kit is being planned where 65nm is traditional rule based, but for 40nm and 28nm the rules are model based in order to accommodate both design and physical effects. The iDFM kits will include compliance tables of which tool and who does what (design, vs layout vs litho) and include litho and CMP rules.

The iPDK libraries are based on Python, and currently are being supported by Synopsys, Ciranova, Springsoft and Magma flows. They support the standard tech files which are fixed per process. For Place and Route tools - there is a list of qualified tools that use the libraries and there is also a support kit including the iRCx and iDRC packages to insure the major 4 P&R tools (Cadence, Synopsys, Magma, Mentor) can run. They also introduced reference flow 10.0 which is for 28nm

